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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,476	08/30/2001	Cliff Zitlaw	400.125US01	9314
27073	7590	03/03/2005	EXAMINER	
LEFFERT JAY & POLGLAZE, P.A. P.O. BOX 581009 MINNEAPOLIS, MN 55458-1009			CHOI, WOO H	
			ART UNIT	PAPER NUMBER
			2186	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/943,476

Applicant(s)

ZITLAW, CLIFF

Examiner

Woo H. Choi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 6, 16, 19 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Each of the above claims recites the limitation “dedicated bus.” The original disclosure does not support this limitation. The closest support for this limitation can be found on page 14, paragraph 16, where the specification discloses that “data transfer is direct from the flash to the SDRAM via a **direct memory bus 212.**” The specification is silent as to whether this direct memory bus is dedicated or not.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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4. Claims 1 – 3, 5, 11, 12, 15, 18 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Baltz (US Patent No. 6,058,474, hereinafter “Baltz”).

5. With respect to claims 1 and 21, Baltz discloses a processing system (figure 8) comprising:

- a processor (10);
- a volatile memory device (23 and 100) coupled to communicate with the processor; and
- a non-volatile memory device (671) coupled to the processor and connected to the volatile memory device, wherein the non-volatile memory device transfers data directly to the volatile memory device during power-up without intervention by any other device (col. 7, lines 46 – 60, see also abstract, see Response to Argument section for further discussion of “without intervention” limitation).

6. With respect to claim 2, the volatile memory device initiates the data transfer in response to a reset signal (abstract).

7. With respect to claim 3, the volatile memory device provides a system reset signal to the processor after the data is transferred from the non-volatile memory device (col. 7, lines 56 – 60).

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8. With respect to claim 5, the volatile memory device initiates the data transfer in response to a reset signal provided by an external reset controller (figures 1A, 4A, 7, 8, reset signal 76 comes from an external source).

9. With respect to claim 11, Baltz discloses a processor system power-up method comprising:

detecting a power-up condition and providing a reset signal to a synchronous memory (abstract and col. 1, lines 25 – 29);

initiating a direct data transfer from a non-volatile memory to the synchronous memory, without intervention from any other device, in response to the reset signal (abstract); and

providing a system reset signal from the synchronous memory to a processor upon completion of the direct data transfer (col. 7, lines 56 – 60).

10. With respect to claims 12, the synchronous memory device is an SDRAM (col. 6, lines 7 – 8).

11. With respect to claim 15, the method further comprises loading the non-volatile memory with the processor prior to detecting the power-up condition (figure 8, 671, EPROM is loaded with a boot code prior to the power-up).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 4, 6 – 9, 14, 16 – 19, rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Harari *et al.* (US Patent No. 6,266,724, hereinafter “Harari”).

Baltz discloses a method of improving a processor system power-up comprising:

detecting a power-up condition with a reset controller and providing a reset signal to an SDRAM;

using the SDRAM, initiating a direct data transfer from an EPROM memory to the SDRAM, over a dedicated bus (figure 8, bus 73 appears to be dedicated for direct transfer of data from memories) in response to the reset signal via a bus without intervention by any other device; and

providing a system reset signal from the SDRAM to a processor after the data has been transferred (see the rejections above).

However, Baltz does not specifically disclose the use of a flash memory for non-volatile memory coupled via a serial bus. On the other hand, Harari discloses a processor system that loads data from a flash memory (figure 7) via a serial bus (col. 7, Lines 34 – 36).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Harari before him at the time the invention was made, to use the flash memory and decompression teachings of the computer system that loads data from a flash EPROM of Harari in the computer system that loads data from an EPROM of Baltz, in order to provide a removable PC card that can accommodate components offloaded from the host system to minimize the size and cost of the host system and to provide flexibility in system configuration (Harari, col. 3, 31 – 35).

14. With respect to claims 18, the synchronous memory device is an SDRAM (col. 6, lines 7 – 8).

15. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Shin (US Patent No. 6,735,669).

Baltz discloses all of the limitations of the parent claim as discussed above. However, Baltz does not specifically disclose the use of a RDRAM. On the other hand Shin discloses that a RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Shin before him at the time the invention was made, to use the lower power

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consumption RDRAM teachings of Shin in the computer system of Baltz, in order to reduce the overall system power consumption. Reduce power consumption is especially important in battery operated portable computer systems.

16. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Harari as applied to claims 6 and 19 and further in view of Shin.

Baltz and Harati disclose all of the limitations of claims 6 and 19 as discussed above. However, Baltz and Harati do not specifically disclose the use of a RDRAM. On the other hand Shin discloses that a RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz, Harati and Shin before him at the time the invention was made, to use the lower power consumption RDRAM teachings of Shin in the computer system of Baltz and Harati, in order to reduce the overall system power consumption. Reduce power consumption is especially important in battery operated portable computer systems.

Response to Arguments

17. In view of the terminal disclaimer filed on January 5, 2005, all double patenting rejections are withdrawn.

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18. Applicant's arguments filed February 3, 2005, have been fully considered but they are not persuasive. First of all, the Examiner notes that Applicant has not shown or argued that the newly added limitations are properly supported by the original disclosure. Nevertheless, the Examiner finds that there is adequate implicit support for the limitation "without intervention" since the specification discloses (page 2, paragraph 6) that "the flash memory device transfers data **directly** to the synchronous memory device." The Examiner's opinion is that direct transfer implies no intervention. If Applicant disagrees with the Examiner, Applicant must present rebuttal arguments and either explicit or inherent support for all newly added limitations in the next reply.

19. Applicant seems to be arguing that because Baltz discloses transfer of data from a non-volatile memory to a volatile memory using a DMA circuitry it does not teach the claimed invention. The Examiner disagrees. DMA circuitry is not a separate device in the sense the term device is used in the claim. The volatile memory device disclosed by Applicant includes various control circuitries as shown in figure 1 and must include others, for example, control circuit for the serial port 132, bus interface circuits etc..., that are not shown to function properly. DMA circuitry disclosed by Baltz is a memory control circuit that controls transfer of data to and from the memory just as various control circuits included in the claimed devices control transfer of data to and from the claimed memory devices. The DMA circuitry of Baltz controls data transfer but does not intervene. The actual transfer is direct from memory to memory. The acronym DMA stands for "**direct** memory access", i.e., without intervention.

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20. As to applicant's other arguments, they fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Woo H. Choi
March 1, 2005